

ABSTRACT OF THE DISCLOSURE

A method is provided for eliminating a polish stop layer from a polishing process.

In particular, a method is provided which may include polishing an upper layer of a
5 semiconductor topography to form an upper surface at an elevation above an underlying
layer, wherein the upper surface does not include a polish stop material. Preferably, the
upper surface of the topography formed by polishing is spaced sufficiently above the
underlying layer to avoid polishing the underlying layer. The entirety of the upper surface
may be simultaneously etched to expose the underlying layer. In an embodiment, the
10 underlying layer may comprise a lateral variation in polish characteristics. The method
may include using fixed abrasive polishing of a dielectric layer for reducing a required
thickness of an additional layer underlying the dielectric layer. Such a method may be
useful when exposing an underlying layer is desirable by techniques other than polishing.

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